IN THE CLAIMS:

Please cancel claims 1-3 and 10-12 without prejudice or disclaimer as to the subject matter contained therein.

Please amend the claims as shown below in the listing of claims.

Claims 1-3 (Cancelled)

4. (Currently amended) ~~The scheduler unit as recited in claim 3,~~ A scheduler unit for an input/output node of a computer system comprising:

a first buffer circuit coupled to receive control commands from a first source, wherein said first buffer circuit includes a first plurality of buffers for storing selected control commands;

a second buffer circuit coupled to receive control commands from a second source, wherein said second buffer circuit includes a second plurality of buffers for storing selected control commands; and

an arbitration circuit coupled to said first buffer circuit and to said second buffer circuit, said arbitration circuit is configured to arbitrate between said control commands stored in said first buffer circuit and said control commands stored in said second buffer circuit;

wherein the outcome of selected arbitration cycles is dependent upon a number of times in which a control command from a given one of said buffers is blocked due to an unavailable destination;

wherein said arbitration circuit includes a first arbitration unit configured to arbitrate between said selected control commands stored within said first plurality of buffers and a second arbitration unit configured to arbitrate between said selected control commands stored within said second plurality of buffers;

wherein said arbitration circuit further includes a fairness unit coupled to said first arbitration unit and said second arbitration unit, said fairness unit is configured to determine a current transaction request rate for said input/output node and to establish an arbitration priority dependent upon said current transaction request rate.

5. (Original) The scheduler unit as recited in claim 4, wherein said arbitration circuit further includes a starvation unit coupled to said fairness unit, wherein said starvation unit is configured to count said number of times in which a control command from a given one of said buffers is blocked due to an unavailable destination.

6. (Original) The scheduler unit as recited in claim 5, wherein said starvation unit is further configured to store a value corresponding to a maximum allowable number of times in which a control command from a given one of said buffers is blocked due to an unavailable destination.

7. (Original) The scheduler unit as recited in claim 6, wherein said arbitration circuit is further configured to select said blocked control command from a given one of said buffers in response to said value corresponding to a maximum allowable number is equal to said count of said number of times in which a control command from a given one of said buffers is blocked.

8. (Currently amended) The scheduler unit as recited in claim [1] 4, wherein said unavailable destination is a destination buffer.

9. (Currently amended) The scheduler unit as recited in claim [1] 8, wherein said arbitration circuit is further configured to determine whether storage space is available within said destination buffer.

Claims 10-12 (Cancelled)

13. (Currently amended) ~~The control unit as recited in claim 12,~~ A control unit for an input/output node of a computer system comprising:

a scheduler unit including:

a first buffer circuit coupled to receive control commands from a first source, wherein said first buffer circuit includes a first plurality of buffers for storing selected control commands;

a second buffer circuit coupled to receive control commands from a second source, wherein said second buffer circuit includes a second plurality of buffers for storing selected control commands; and

an arbitration circuit coupled to said first buffer circuit and to said second buffer circuit, said arbitration circuit is configured to arbitrate between said control commands stored in said first buffer circuit and said control commands stored in said second buffer circuit;

wherein the outcome of selected arbitration cycles is dependent upon a number of times in which a control command from a given one of said buffers is blocked due to an unavailable destination;

wherein said arbitration circuit includes a first arbitration unit configured to arbitrate between said selected control commands stored within

said first plurality of buffer and a second arbitration unit configured to arbitrate between said selected control commands stored within said second plurality of buffers; and

wherein said arbitration circuit further includes a fairness unit coupled to said first arbitration unit and said second arbitration unit and configured to determine a current transaction request rate for said input/output node and to establish an arbitration priority between said first arbitration unit and said second arbitration unit based on said current transaction request rate.

14. (Original) The control unit as recited in claim 13, wherein said arbitration circuit further includes a starvation unit coupled to said fairness unit, wherein said starvation unit is configured to count said number of times in which a control command from a given one of said buffers is blocked due to an unavailable destination.

15. (Original) The control unit as recited in claim 14, wherein said starvation unit is further configured to store a value corresponding to a maximum allowable number of times in which a control command from a given one of said buffers is blocked due to an unavailable destination.

16. (Original) The control unit as recited in claim 15, wherein said arbitration circuit is further configured to select said blocked control command from a given one of said buffers in response to said value corresponding to a maximum allowable number is equal to said count of said number of times in which a control command from a given one of said buffers is blocked.

17. (Currently amended) The control unit as recited in claim [10] 13, wherein said unavailable destination is a destination buffer.

18. (Currently amended) The control unit as recited in claim [10] 17, wherein said arbitration circuit is further configured to determine whether storage space is available within said destination buffer.